REMARKS

Claims 1–7 and 27–39 are pending in the present application.

Claims 27–28 and 33 have been amended. Claims 28 was amended solely to rewrite the claim in independent form and to correct an antecedent basis error. Claim 33 were amended solely to correct an antecedent basis defect.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, Second Paragraph (Definiteness)

Claims 1–7 and 28–39 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. This rejection is respectfully traversed.

The standard for definiteness is whether a claim reasonably a apprises those of skill in the art of its scope. MPEP § 2173.02; *In re Warmerdam*, 33 F.3d 1354, 1361, 31 U.S.P.Q.2d 1754, 1759 (Fed. Cir. 1994). Whether the claim leaves unclear the manner in which a feature may be implemented is irrelevant where the claim clearly covers all forms of implementation. *In re Warmerdam*, 33 F.3d 1354, 1361, 31 U.S.P.Q.2d 1754, 1759 (Fed. Cir. 1994). Determining whether a claim is indefinite requires an analysis of whether one skilled in the art would understand the bounds of the claim when read in light of the specification. *Credle v. Bond*, 25 F.3d 1566, 1576, 30 U.S.P.Q.2d 1911, 1919 (Fed. Cir. 1994). The claim is not indefinite if one skilled in the art would have no particular difficulty in determining whether the claimed features

have been implemented. *In re Warmerdam*, 33 F.3d 1354, 1361, 31 U.S.P.Q.2d 1754, 1759 (Fed. Cir. 1994). The claim limitation is sufficient if it enables those skilled in the art to draw a line between embodiments falling within the scope of the claim and those which do not. *In re Marosi*, 710 F.2d 799, 802-03, 218 U.S.P.Q. 289, 292 (Fed. Cir. 1983).

The Office Action states that various claim limitations within the independent claims are indefinite. However, the Office Action does not explain how those limitations are indefinite, or why those skilled in the art would be unable to determine whether the corresponding feature has been implemented.

Therefore, the rejection of claims 1–7 and 28–39 under 35 U.S.C. § 112, second paragraph has been overcome.

1. **35 U.S.C. § 102 (Anticipation)**

Claims 27–28 and 33–34 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,273,914 to *Miyajima et al.* Claims 27–30 and 32 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,766,991 to *Chen*. This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed

invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Independent claim 27 recites that first and second sidewalls overlying a portion of the channel and portions of the source and drain regions of the p-channel transistor, in combination with an n-channel transistor having lightly doped source/drain regions. Such a feature is not shown or suggested by the cited references. *Miyajima et al* does not teach such a feature, while *Chen* teaches removing the (second) silicon nitride sidewalls 76 through 79 prior to implanting lightly doped regions for the n-channel transistor. *Chen*, column 6, lines 64–65.

Claim 28 recites that the p-channel gate electrode is smaller than a minimum channel length for the p-channel transistor. Such a feature is not taught by the cited references. Both references depict structures in which the gate electrode is shorter than the channel length, but neither reference teaches that the gate electrode is shorter than the minimum viable channel length for the fabrication process utilized.

Independent claim 33 recites a gate electrode for the p-channel transistor having a width smaller than the minimum channel length for the p-channel transistor and covered by at least one conformal insulating layer with a thickness that, taken twice (once on each side of the gate electrode) and added to the width of the gate electrode, exceeds the minimum channel length. In the present invention, implantation of the source/drain regions for the p-channel transistor are masked by the gate electrode and an overlying conformal insulating layer. A subsequent

diffusion drives the impurities under sidewall spacers formed from the insulating layer Such a feature is not shown or suggested by either reference.

Therefore, the rejections of claims 27–30 and 32–34 under 35 U.S.C. § 102 have been overcome.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

Claims 27–28 and 33 were amended herein as follows:

27. (amended) A CMOS integrated circuit structure, comprising:

an n-channel transistor including lightly doped source and drain regions within a p-type region of a substrate; and

a p-channel transistor without lightly doped source and drain regions within an n-type region of the substrate, the p-channel transistor including:

a gate electrode having a width less than a channel length of a channel for the p-channel transistor; and

first and second sidewall spacers adjacent opposing sides of the gate electrode and overlying [at least] a portion of the channel for the p-channel transistor and portions of source and drain regions for the p-channel transistor.

28. (amended) [The]A CMOS integrated circuit structure[of claim 27], comprising:

an n-channel transistor including lightly doped source and drain regions within a p-type region of a substrate; and

a p-channel transistor without lightly doped source and drain regions within an n-type region of the substrate, the p-channel transistor including:

a gate electrode having a width less than a channel length of a channel for the p-channel transistor; and

first sidewall spacers adjacent opposing sides of the gate electrode and overlying at least a portion of the channel for the p-channel transistor and portions of source and drain regions for the p-channel transistor,

wherein the width of the gate electrode is less than [the]a minimum channel length required for the p-channel transistor.

33. (amended) An intermediate structure for use in forming a CMOS integrated circuit, comprising:

a p-type region for an n-channel transistor including lightly doped source and drain regions;

an n-type region for a p-channel transistor without lightly doped source and drain regions;

a gate electrode overlying a portion of the n-type region, the gate electrode having a width less than a minimum channel length required for the p-channel transistor; and

[an]at least one conformal insulating layer over a top and sides of the gate electrode, the insulating layer having a thickness which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds [the]a minimum channel length required for the p-channel transistor.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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